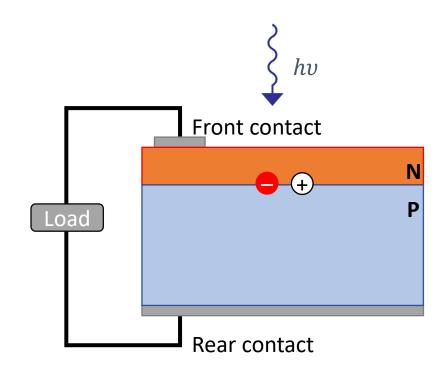


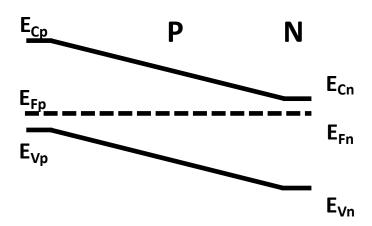
# **Energy Conversion by Semiconductor Devices**

Jun-Ho YUM

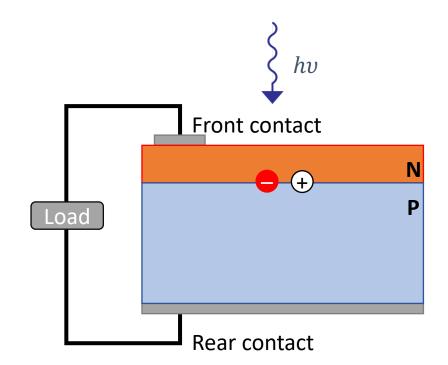
junho.yum@epfl.ch

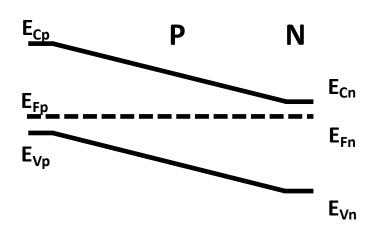
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- The p region is lightly doped so that most of the depletion region lies in the p side.
- Main two processes: carrier generation and carrier collection.
- Electron-hole pairs are generated by the incident photon  $> E_g$ . The electron-hole pairs exist, on average, for a length of time equal to the minority carrier lifetime before they recombine.
- The carriers are separated by the E-field existing at the p-n junction.



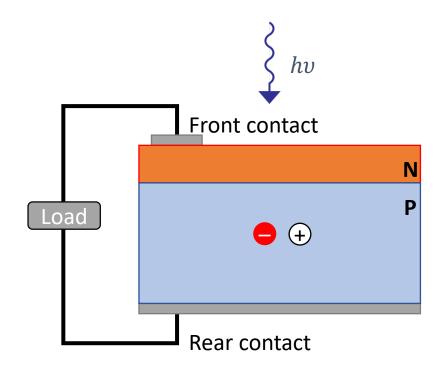


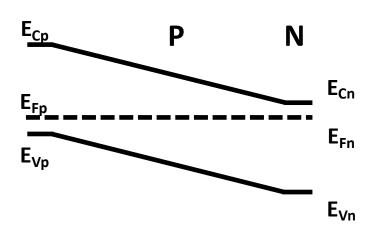
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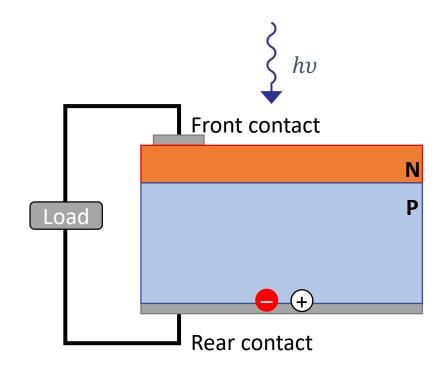


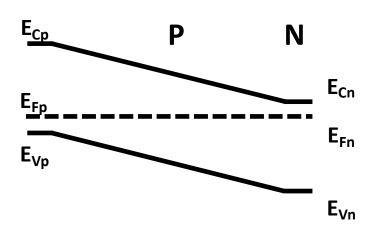
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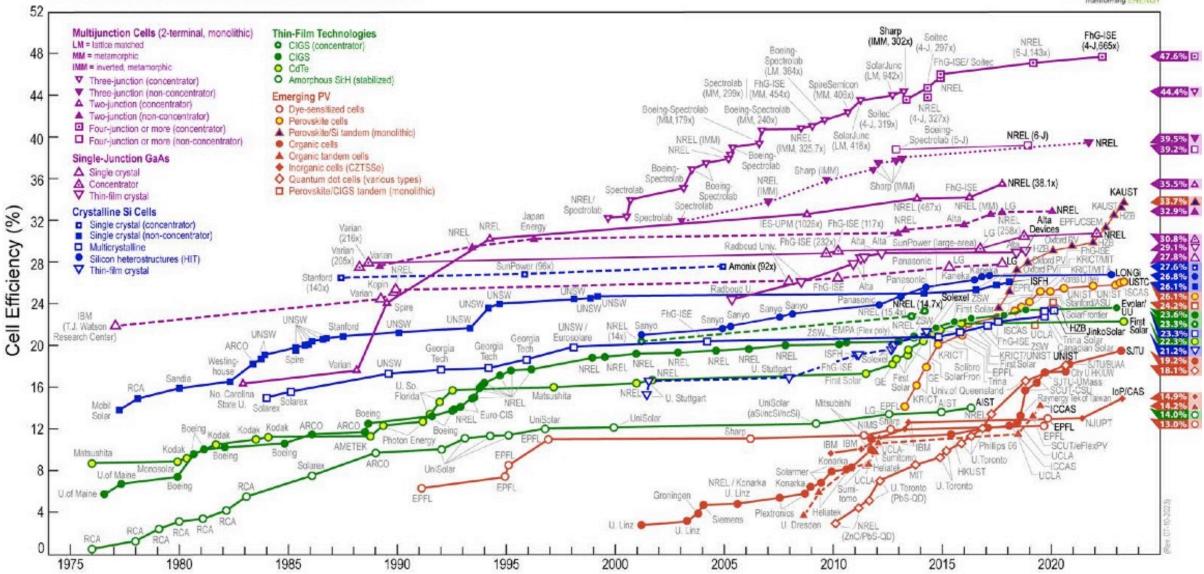




### **EPFL** NREL Best Research-Cell Efficiencies

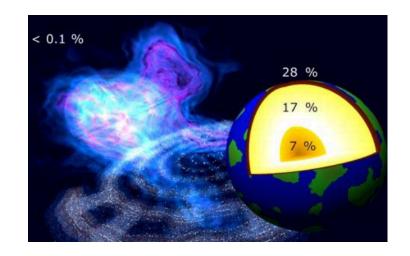
#### **Best Research-Cell Efficiencies**



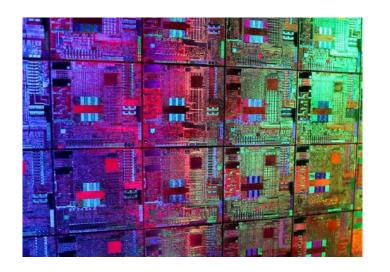


# **EPFL** Silicon Solar Cell

Si has suitable Eg, 1.12 eV
Doing is possible
Abundant and non-toxic
Mostly used in microelectronics

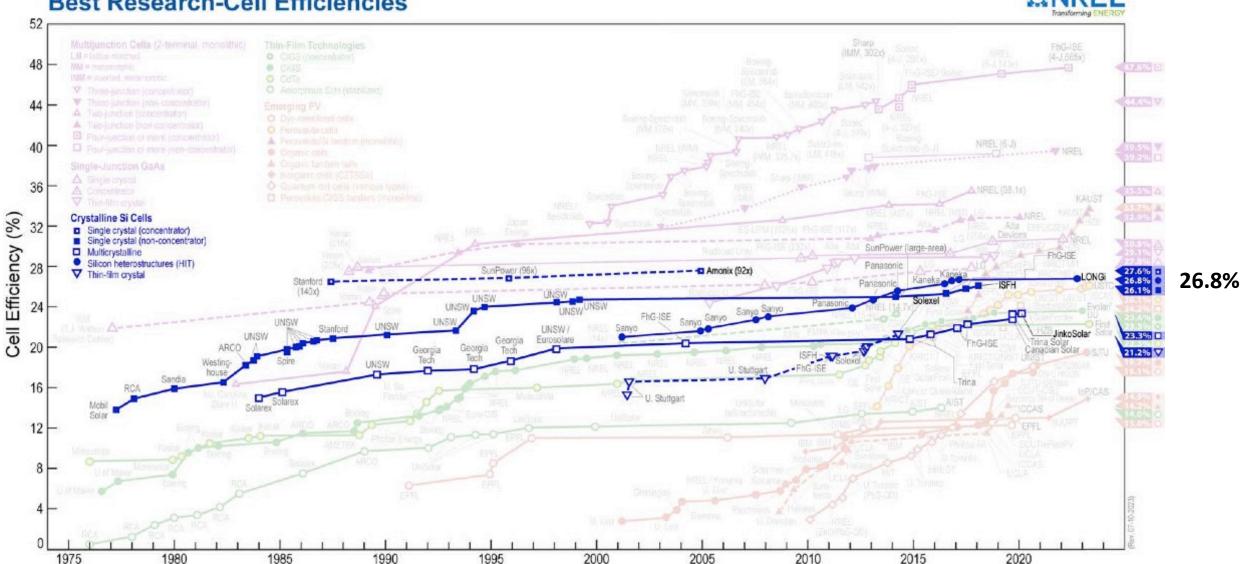






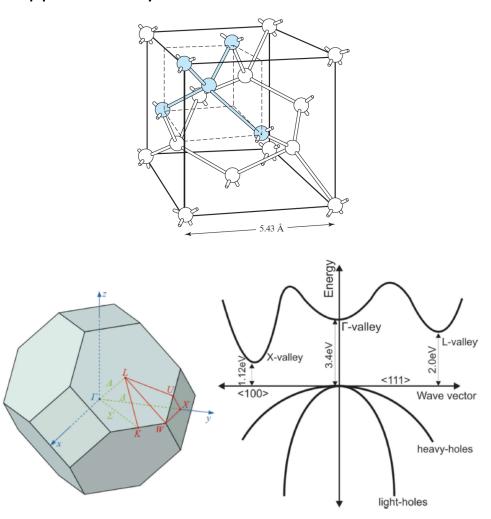
# **EPFL** Type of Silicon for Solar Cells

#### **Best Research-Cell Efficiencies**

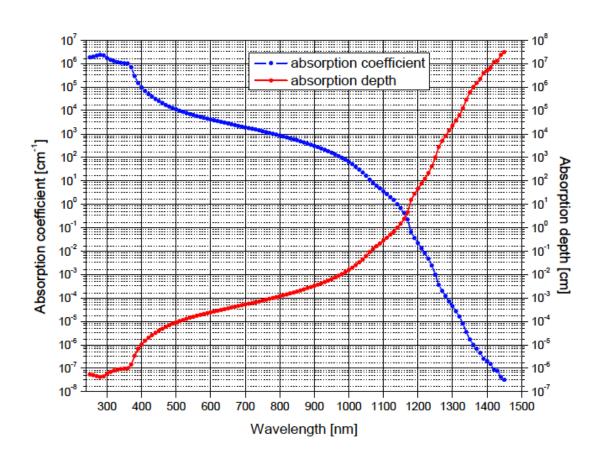




Bond angle is 109°28′ and bond length is approximately 2.35 Å.



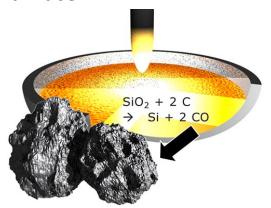
#### Indirect band gap is 1.12 eV

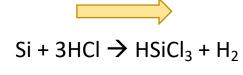


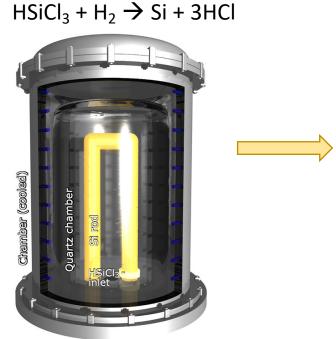
### **EPFL** From Sand to Silicon Single Crystal

Purification of Silicon by distillation (Siemens Process)

Reduction of SiO<sub>2</sub> with carbon to metallurgical grade silicon (>98%) in an electric arc furnace







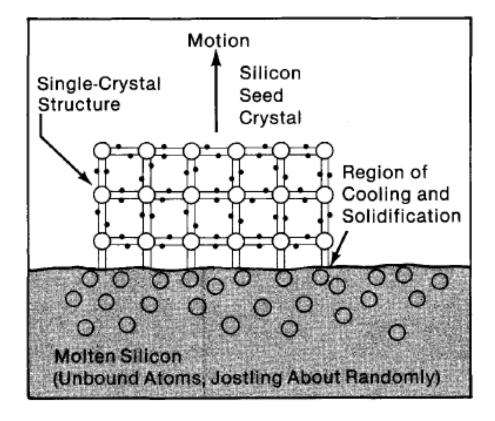
Electronic grade poly silicon  $(9N, impurities < 10^{14} cm^{-3})$ 

#### Czochralski (Cz) Technique

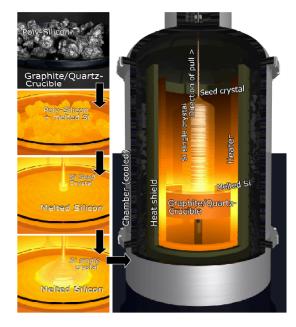


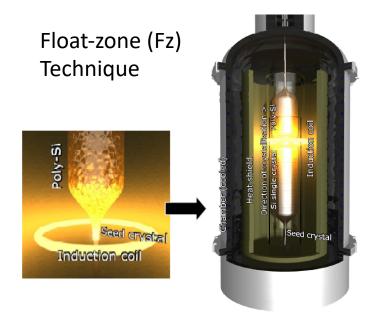


# **EPFL** From Sand to Silicon Single Crystal



#### Czochralski (Cz) Technique





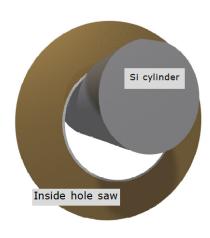
10

# **EPFL** From Single Crystal to Polished Wafer

# oni Single Crystal to Folished Waler

#### Grinding

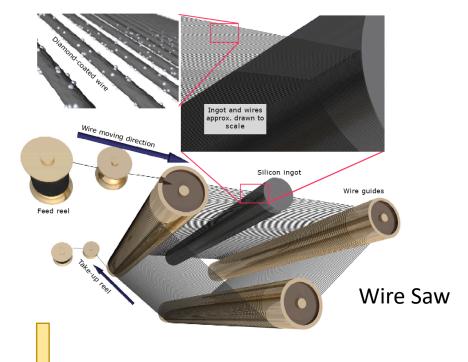


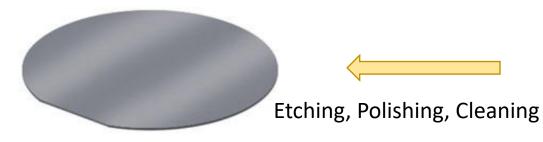


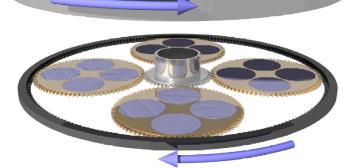
Inside Hole Saw

Schema of a wafer

#### Dicing







Lapping

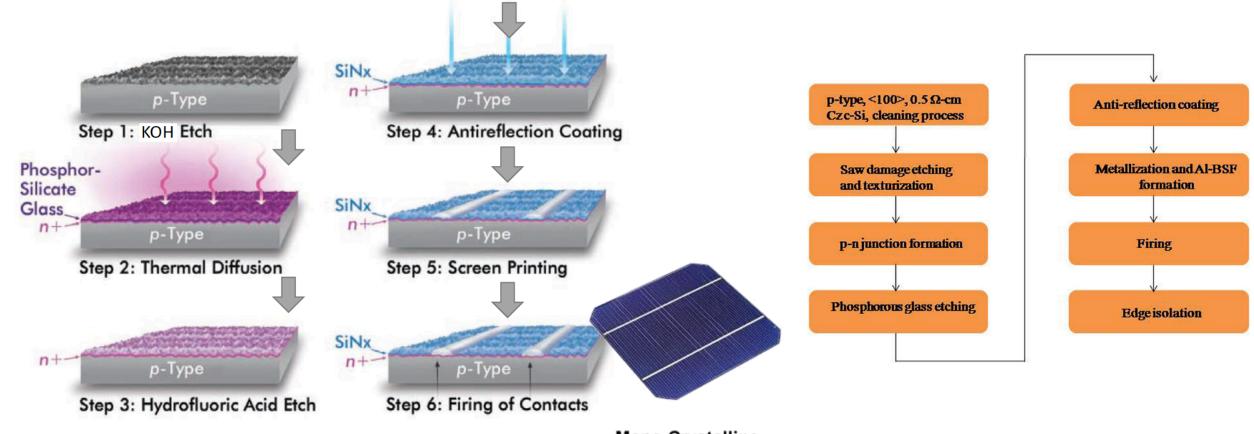
#### **EPFL**

### Single Crystalline Si Solar Cell Cell Fabrication Technologies

Screen Printed Solar Cells: <a href="https://www.pveducation.org/pvcdrom/manufacturing-si-cells/screen-printed-solar-cells">https://www.pveducation.org/pvcdrom/manufacturing-si-cells/screen-printed-solar-cells</a>

Buried Contact Solar Cells: <a href="https://www.pveducation.org/pvcdrom/manufacturing-si-cells/buried-contact-solar-cells">https://www.pveducation.org/pvcdrom/manufacturing-si-cells/buried-contact-solar-cells</a>

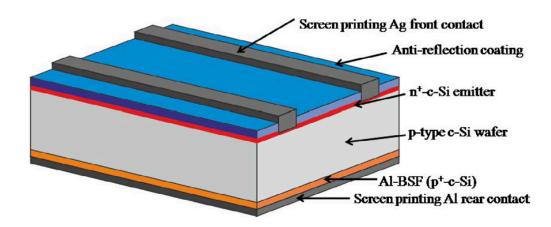
High Efficiency Solar Cells: <a href="https://www.pveducation.org/pvcdrom/manufacturing-si-cells/high-efficiency-solar-cells">https://www.pveducation.org/pvcdrom/manufacturing-si-cells/high-efficiency-solar-cells</a>

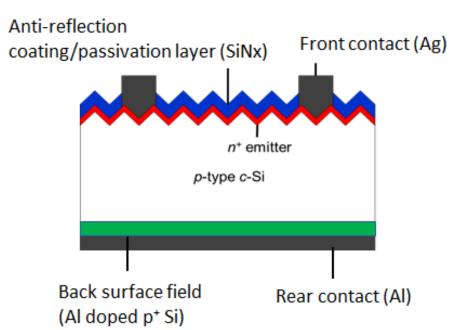




### Single Crystalline Si Solar Cells Architecture

Conventional Si Solar Cell: Al-back surface field (BSF) solar cell





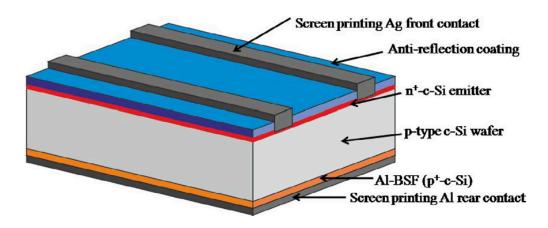
- At the rear side, a heavily Al-doped p<sup>+</sup>-region in ptype c-Si forms a high-low (p<sup>+</sup>/p) junction known as Al-BSF.
- The potential barrier at the high-low (p+/p) junction drives electrons away from reaching the back electrode and towards the pn junction (Reduced surface recombination velocity (SRV))  $\rightarrow$  Increase in  $V_{oc}$  and  $J_{sc}$ .

p-SC	p+-SC



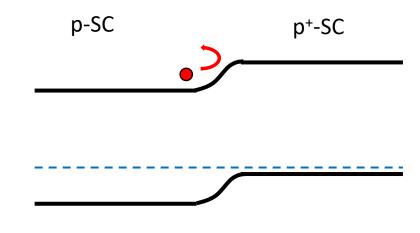
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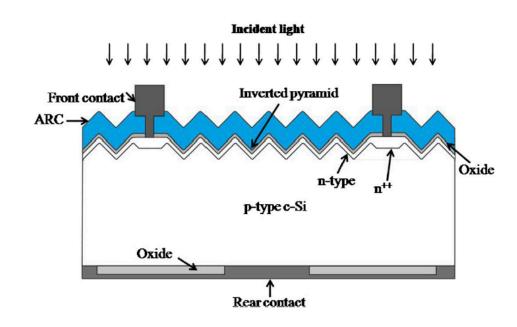
Anti-reflection Front contact (Ag) coating/passivation layer (SiNx) *n*+ emitte p-type c-Si Back surface field Rear contact (AI) (Al doped p<sup>+</sup> Si)

- At the rear side, a heavily Al-doped p<sup>+</sup>-region in ptype c-Si forms a high-low (p+/p) junction known as Al-BSF.
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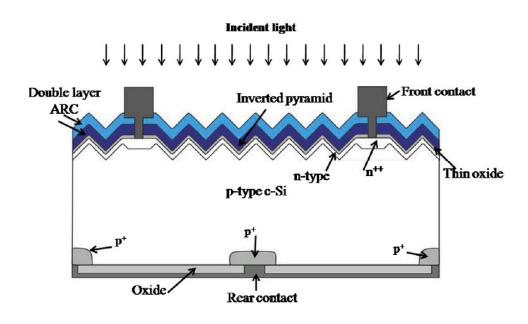


### **EPFL** PERC and PERL Solar Cells

High Efficiency Solar Cell: passivated emitter rear contact (PERC) and passivated emitter rear locally-diffused (PERL) solar cell



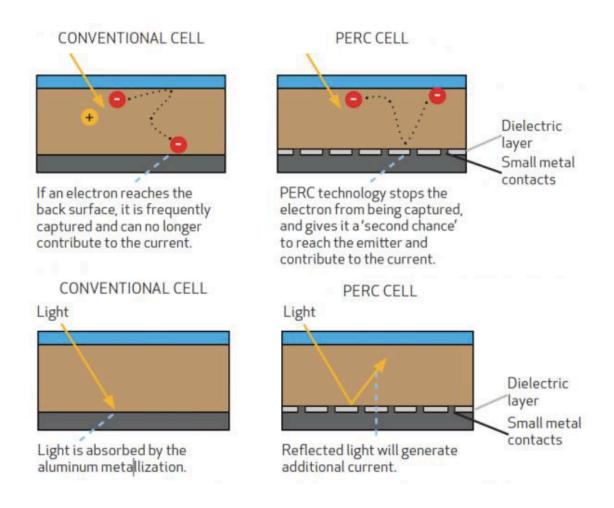
Rear side dielectric passivation layer ( $Al_2O_3$ ): reduced surface recombination and improved reflection.

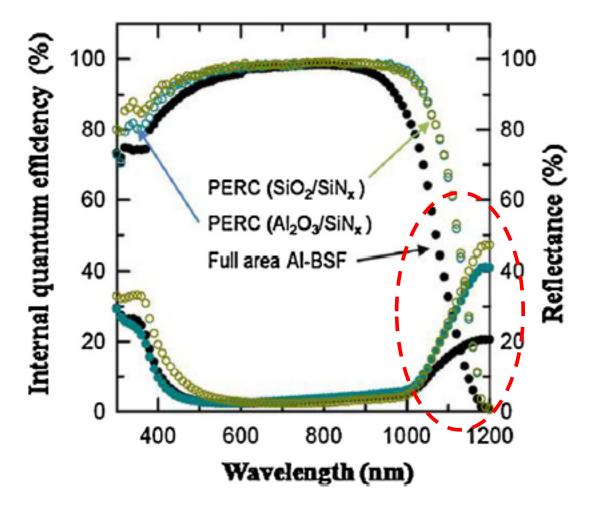


Electric field in the BSF region between p+/p junction drives electrons away towards the pn junction and reduces surface recombination at the defective metal/c-Si interface.

#### 21.2% with PERC and 25% with PERL

### **EPFL** PERC and PERL Solar Cells

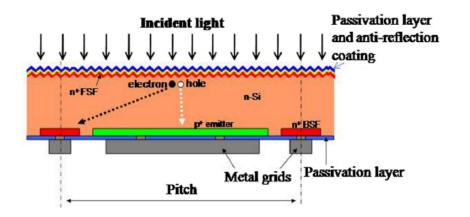




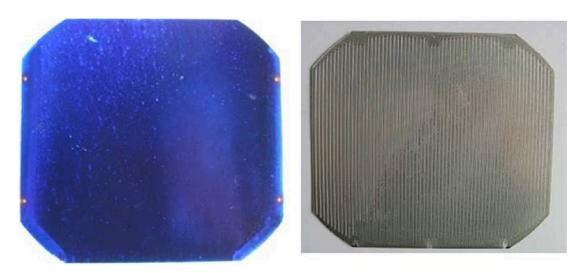
Dullweber T. et al., Prog Photovolt: Res Appl; 20:630–8 (2012)

### **EPFL** IBC c-Si Solar Cells

Interdigitated back contact (IBC) c-Si solar cells



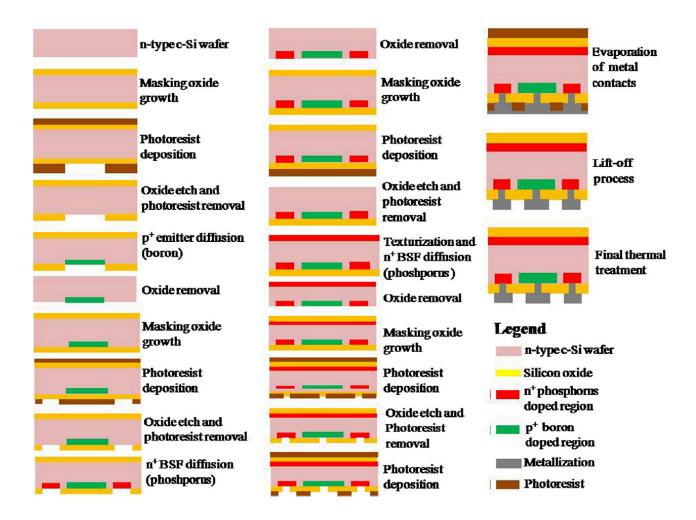
- Major advantage: No front side metallization grid  $\rightarrow$  Zero shading losses  $\rightarrow$  High  $J_{sc}$
- Passivation and light trapping properties can be optimized for the front side
- No limit for the width and thickness of metallization on the back side: Reduced series R
- Advantageous for the module manufacturing because of co-planar interconnection of the back-contact



Grid less front side (147.4 cm<sup>2</sup>)

Rear side

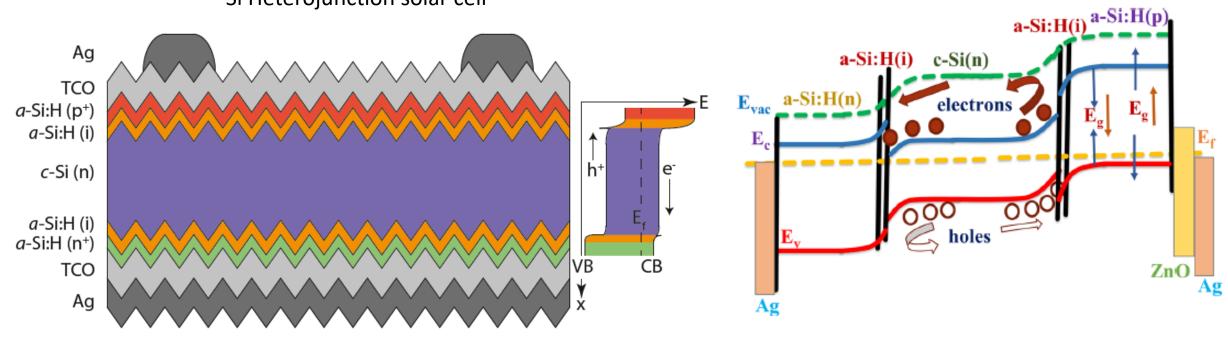
### **EPFL** IBC c-Si Solar Cells



- The complexity of the processing technology: Example of a complex laboratory scale process flow for the IBC solar cell processing using photolithography and high-temperature diffusion processes.
- Photolithography is however not a cost-effective process for mass production in the photovoltaic industry.
- High accuracy masking steps are required to avoid shunting between p-type and n-type electrodes.
- Highly pure, lightly doped Fz c-Si wafers with diffusion length at the least four times higher than the thickness of the c-Si wafer and the lifetime of 1 3 ms are required.







Wolf et al., Green, 2.7 – 24 (2012)

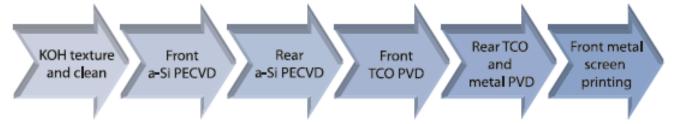
V. Kanneboina, J. Comp. Electronics, 20:344 (2021)

- Doped (n or p) a-Si:H over-layers are used to form junctions as electron and hole collectors, allowing the fabrication of nearly recombination-free contacts.
- Long carrier lifetime by a-Si:H over-layers
- Charges trickle through the buffer layers sufficiently slowly to build up a high voltage e.g > 730 mV.

### **EPFL** Si

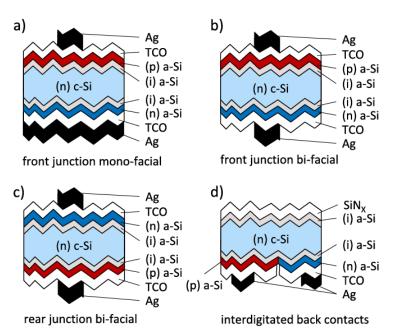
### **Silicon Heterojunction Solar Cells**

Basic process steps for Si Heterojunction solar cell: low temperature process <200 °C



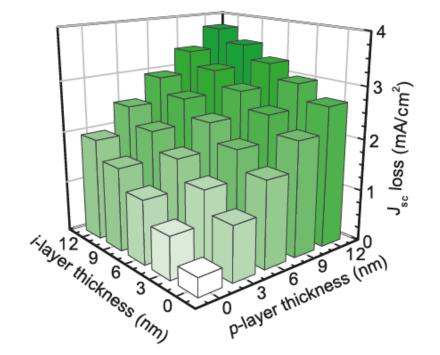
Wolf et al., Green, 2.7 - 24 (2012)

#### Device architectures for SHJ solar cells.



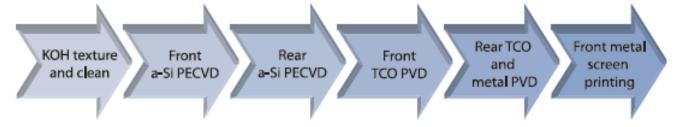
Haschke et al., Solar Energy Mater. Solar Cells, 187. 140 – 153 (2018)

Estimate of the losses in  $J_{sc}$  below 600 nm associated with increasing intrinsic and p-type layer thicknesses: bandgap of a-Si:H (1.7–1.9 eV)



# **EPFL** Silicon Heterojunction Solar Cells

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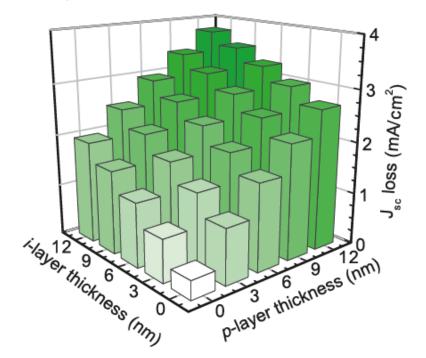


Wolf et al., Green, 2.7 - 24 (2012)

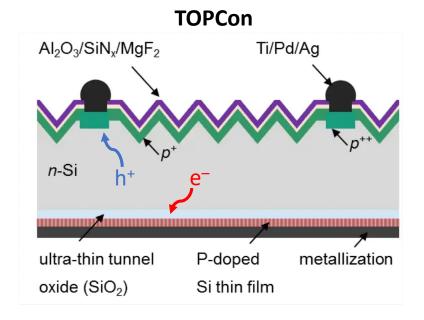
Estimate of the losses in  $J_{sc}$  below 600 nm associated with increasing intrinsic and p-type layer thicknesses: bandgap of a-Si:H (1.7–1.9 eV)

#### Solution!

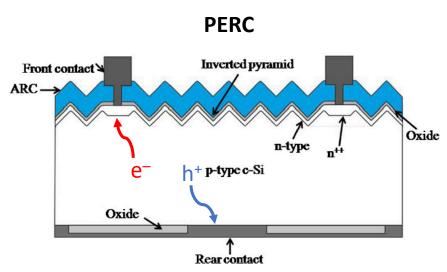
- Improving TCO transparency.
- Replacing a-Si:H with microcrystalline Si, which has features a higher doping.
- Combination with IBC structure.
- Thinner wafer (general trend for all c-Si PV technologies) possible to further increase  $V_{oc}$ .

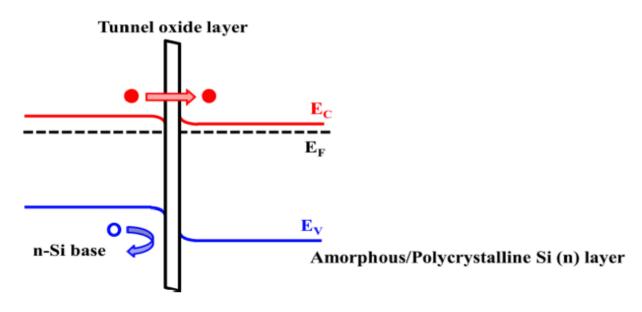


### **EPFL** TOPCon Silicon Solar Cell

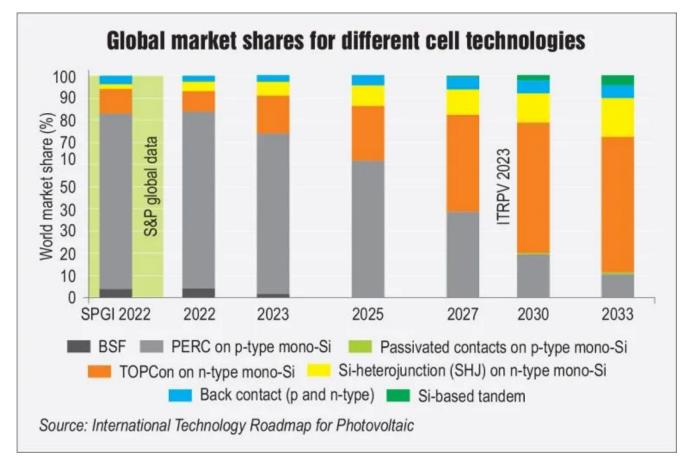


- The term TOPCon stands for Tunnel Oxide Passivated Contact and the architecture was presented by researchers at the Fraunhofer Institute for Solar Energy Systems in Freiburg in 2013.
- A very thin layer of silicon oxide (just a few nanometers) is applied to the surface of the solar cell and the SiO₂ layer passivates the surface, i.e. low surface recombination.
- However, the layer is so thin that the current can "tunnel through".





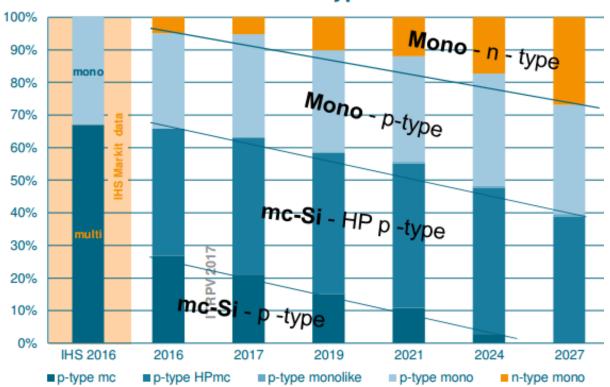
# **EPFL** Trend for Single Crystalline Si Solar Cells



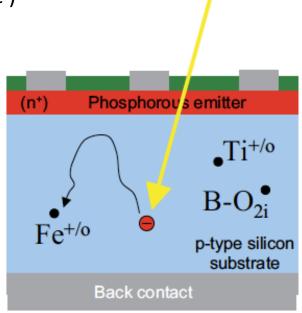
	PERC	TOPCon	НЈТ	IBC
Efficiency in mass production	23.50 %	24.80 %	25.80 %	25.00 %
Efficiency in lab	24.50 %	26.40 %	26.81 %	25.20 %

# **EPFL** Trend for Single Crystalline Si Solar Cells

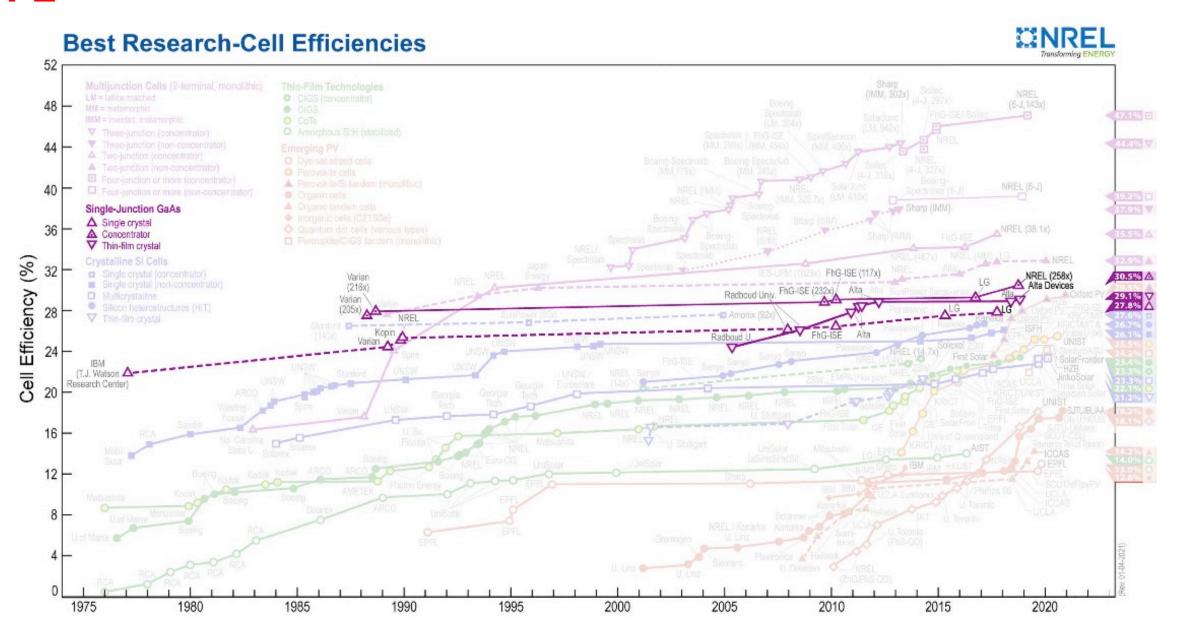
#### Trend: share of c-Si material types



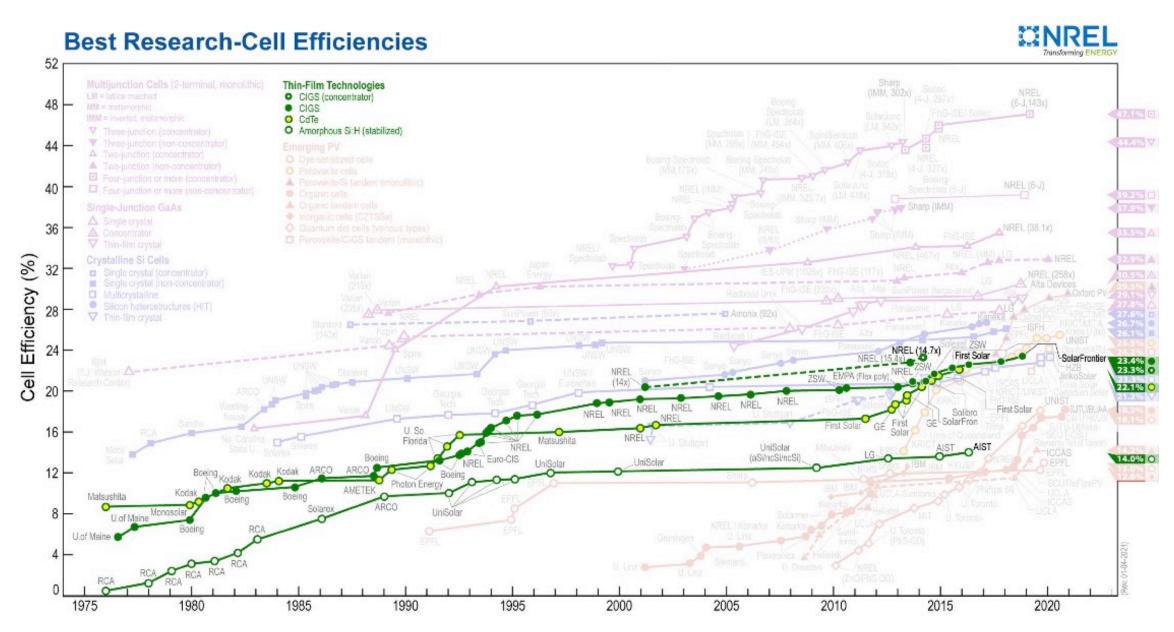
- Boron doped p-type Cz water: Boron (dopant) and oxygen (growth process impurity) forms a boron-oxygen related metastable defect upon illumination
  - → Solution: Boron to Gallium dopant
    FZ instead of Cz
    Regeneration process to remove the defect
- Transition metal defects, Fe in p-type wafers have an increased capture rate for minority carriers in p-type wafers (e<sup>-</sup>)



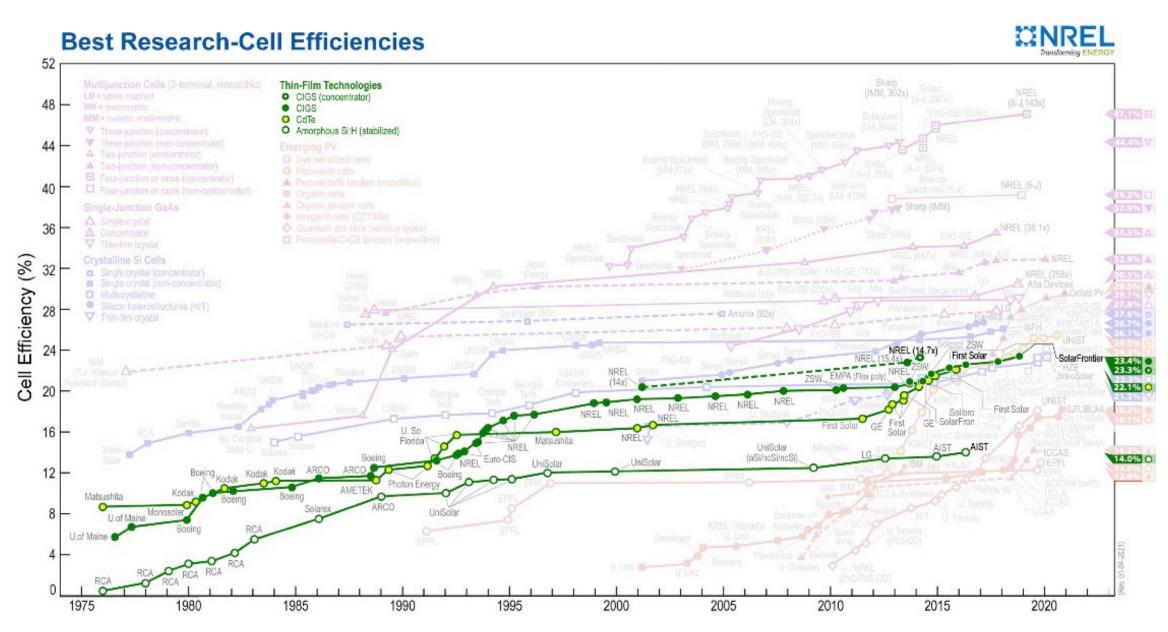
## **EPFL** III-V Semiconductors: GaAs



## **EPFL** II-VI Semiconductors: CdTe



## **EPFL** CIGS Thin Film Solar Cells



# **EPFL** Efficiency Comparison of Technologies

